CLAIMS

We claim:

1. A method of forming a double-gated transistor, comprising the steps of:

a) providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI oxide layer and an upper SOI silicon layer;

b) forming a top oxide layer over the SOI structure;

c) forming a first top dummy layer over the top oxide layer;

d) patterning:

I) the first top dummy layer;

II) the top oxide layer; and

III) the upper SOI silicon layer to form a patterned first top dummy layer /top oxide layer /upper SOI silicon layer stack having exposed side walls; the patterned upper SOI silicon layer including a source region and a drain region connected by a channel portion;

e) forming a rounded oxide layer over the exposed side walls of the patterned upper SOI silicon layer;; the formation of the rounded oxide layer also rounding the patterned upper SOI silicon layer;

f) removing the patterned first top dummy layer exposing the patterned top oxide layer;

g) forming a second patterned dummy layer over the exposed patterned top oxide layer and the exposed portions of the upper SOI silicon layer; the second patterned dummy layer having an opening that defines a gate area exposing:

I) a portion of the oxide layer within the gate area;

II) portions of the upper surface of the lower SOI oxide layer within the gate area; and

III) a portion of the rounded oxide layer within the gate area;

h) etching the exposed gate area portions of the upper surface of the lower SOI oxide layer into the lower SOI oxide layer to:

I) form an undercut into the undercut lower SOI oxide layer exposing a bottom portion of the patterned upper SOI silicon layer within the gate area;

II) remove the exposed gate area portion of the oxide layer exposing a top portion of the patterned upper SOI silicon layer within the gate area; and

III) remove the portion of the rounded oxide layer within the gate area exposing a portion of the side walls of the patterned upper SOI silicon layer within the gate area;

i) forming a conformal oxide layer over:

I) the exposed bottom portion of the patterned upper SOI silicon layer within the gate area;

II) the exposed top portion of the patterned upper SOI silicon layer within the gate area; and

x III) the exposed portion of the side walls of the patterned upper SOI silicon layer within the gate area;

j) forming a gate within the second patterned dummy layer opening; the gate including an upper gate above the patterned upper SOI silicon layer 14' within the gate area and a lower gate under the upper SOI silicon layer within the gate area; and

k) removing the second patterned dummy layer to form the double-gated transistor.

2. The method of claim 1, wherein the structure is a semiconductor substrate.

3. The method of claim 1, wherein the structure is comprised of silicon or germanium.

4. The method of claim 1, wherein the lower SOI oxide layer has a thickness of from about 1000 to 5000Å; the upper SOI silicon layer has a thickness of from about 300 to 2000Å; the first dummy layer has a thickness of from about 450 to 1050Å; the top oxide layer has a thickness of from about 90 to 110Å; the rounded oxide layer has a thickness of from about 80 to 550Å; the second patterned dummy layer has a thickness of from about 1000 to 3000Å; and the conformal oxide layer has a thickness of from about 5 to 200Å.

5. The method of claim 1, wherein the lower SOI oxide layer has a thickness of from about 2000 to 4000Å; the upper SOI silicon layer has a thickness of from about 500 to 1500Å; the first dummy layer has a thickness of from about 500 to 1000Å; the top oxide layer has a thickness of from about 95 to 105Å; the rounded oxide layer has a thickness of from about 100 to 500Å; the second patterned dummy layer has a thickness of from about 1500 to 2500Å; and the conformal oxide layer has a thickness of from about 10 to 50Å.

6. The method of claim 1, wherein the undercut is from about 500 to 3000Å deep.

7. The method of claim 1, wherein the undercut is from about 1000 to 2000Å deep.

8. The method of claim 1, wherein the undercut protrudes from about 500 to 3000Å under the second patterned dummy layer opening.

9. The method of claim 1, wherein the undercut protrudes from about 500 to 1000Å under the second patterned dummy layer opening.

10. The method of claim 1, wherein the first dummy layer is comprised of nitride, silicon nitride or silicon oxynitride; the second patterned dummy layer is comprised of nitride, silicon nitride or silicon oxynitride; and the gate is comprised of polysilicon, tungsten, W-Si_x, SiGe or aluminum.

11. The method of claim 1, wherein the first dummy layer is comprised of nitride or silicon nitride; the second patterned dummy layer is comprised of nitride or silicon nitride; and the gate is comprised of polysilicon.

12. The method of claim 1, wherein the patterned first dummy layer is removed using a hot phosphoric acid etch the undercut is formed using a dilute HF etch and the second patterned dummy layer is removed using hot phosphoric acid.

13. The method of claim 1, wherein the rounded oxide layer and the conformal oxide layer are each formed by a growth process.

14. The method of claim 1, including the step of forming source/drain implants into the respective source region and the drain region to form a source and a drain after removal of the second patterned dummy layer.

15. The method of claim 1, including the step of performing:

LDD implants; and

source/drain implants

after removal of the second patterned dummy layer.

16. The method of claim 1, wherein the upper gate has exposed side walls and including the step of forming spacers over the upper gate exposed side walls after removal of the second patterned dummy layer.

17. The method of claim 1, including the further step of then performing a salicidation process.

18. A method of forming a double-gated transistor, comprising the steps of:

a) providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI oxide layer and an upper SOI silicon layer;

b) forming a top oxide layer over the SOI structure;

c) forming a first top dummy layer over the top oxide layer; the first dummy layer being comprised of nitride, silicon nitride or silicon oxynitride;

d) patterning:

I) the first top dummy layer;

II) the top oxide layer; and

III) the upper SOI silicon layer to form a patterned first top dummy layer /top oxide layer /upper SOI silicon layer stack having exposed side walls; the patterned upper SOI silicon layer including a source region and a drain region connected by a channel portion;

e) forming a rounded oxide layer over the exposed side walls of the patterned upper SOI silicon layer;; the formation of the rounded oxide layer also rounding the patterned upper SOI silicon layer;

f) removing the patterned first top dummy layer exposing the patterned top oxide layer;

g) forming a second patterned dummy layer over the exposed patterned top oxide layer and the exposed portions of the upper SOI silicon layer; the second patterned dummy layer having an opening that defines a gate area exposing; the second patterned dummy layer being comprised of nitride, silicon nitride or silicon oxynitride;

I) a portion of the oxide layer within the gate area;

II) portions of the upper surface of the lower SOI oxide layer within the gate area; and

III) a portion of the rounded oxide layer within the gate area;

h) etching the exposed gate area portions of the upper surface of the lower SOI oxide layer into the lower SOI oxide layer to:

I) form an undercut into the undercut lower SOI oxide layer exposing a bottom portion of the patterned upper SOI silicon layer within the gate area;

II) remove the exposed gate area portion of the oxide layer exposing a top portion of the patterned upper SOI silicon layer within the gate area; and

III) remove the portion of the rounded oxide layer within the gate area exposing a portion of the side walls of the patterned upper SOI silicon layer within the gate area;

i) forming a conformal oxide layer over:

I) the exposed bottom portion of the patterned upper SOI silicon layer within the gate area;

II) the exposed top portion of the patterned upper SOI silicon layer within the gate area; and

III) the exposed portion of the side walls of the patterned upper SOI silicon layer within the gate area;

j) forming a gate within the second patterned dummy layer opening; the gate including an upper gate above the patterned upper SOI silicon layer 14' within the gate area and a lower gate under the upper SOI silicon layer within the gate area; the gate being comprised of polysilicon, tungsten, W-Si_x, SiGe or aluminum; and

k) removing the second patterned dummy layer to form the double-gated transistor.

19. The method of claim 18, wherein the structure is a semiconductor substrate.

20. The method of claim 18, wherein the structure is comprised of silicon or germanium.

21. The method of claim 18, wherein the lower SOI oxide layer has a thickness of from about 1000 to 5000Å; the upper SOI silicon layer has a thickness of from about 300 to 2000Å; the first dummy layer has a thickness of from about 450 to 1050Å; the top oxide layer has a thickness of from about 90 to 110Å; the rounded oxide layer

has a thickness of from about 80 to 550Å; the second patterned dummy layer has a thickness of from about 1000 to 3000Å; and the conformal oxide layer has a thickness of from about 5 to 200Å.

22. The method of claim 18, wherein the lower SOI oxide layer has a thickness of from about 2000 to 4000Å; the upper SOI silicon layer has a thickness of from about 500 to 1500Å; the first dummy layer has a thickness of from about 500 to 1000Å; the top oxide layer has a thickness of from about 95 to 105Å; the rounded oxide layer has a thickness of from about 100 to 500Å; the second patterned dummy layer has a thickness of from about 1500 to 2500Å; and the conformal oxide layer has a thickness of from about 10 to 50Å.

23. The method of claim 18, wherein the undercut is from about 500 to 3000Å deep.

24. The method of claim 18, wherein the undercut is from about 1000 to 2000Å deep.

25. The method of claim 18, wherein the undercut protrudes from about 500 to 3000Å under the second patterned dummy layer opening.

26. The method of claim 18, wherein the undercut protrudes from about 500 to 1000Å under the second patterned dummy layer opening.

27. The method of claim 18, wherein the first dummy layer is comprised of nitride or silicon nitride; the second patterned dummy layer is comprised of nitride or silicon nitride; and the gate is comprised of polysilicon.

28. The method of claim 18, wherein the patterned first dummy layer is removed using a hot phosphoric acid etch the undercut is formed using a dilute HF etch and the second patterned dummy layer is removed using hot phosphoric acid.

29. The method of claim 18, wherein the rounded oxide layer and the conformal oxide layer are each formed by a growth process.

30. The method of claim 18, including the step of forming source/drain implants into the respective source region and the drain region to form a source and a drain after removal of the second patterned dummy layer.

31. The method of claim 18, including the step of performing:

LDD implants; and

source/drain implants

after removal of the second patterned dummy layer.

32. The method of claim 18, wherein the upper gate has exposed side walls and including the step of forming spacers over the upper gate exposed side walls after removal of the second patterned dummy layer.

33. The method of claim 18, including the further step of then performing a salicidation process.

34. A method of forming a double-gated transistor, comprising the steps of:

a) providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI oxide layer and an upper SOI silicon layer;

b) forming a top oxide layer over the SOI structure;

c) forming a first top dummy layer over the top oxide layer; the first dummy layer being comprised of nitride or silicon nitride;

d) patterning:

I) the first top dummy layer;

II) the top oxide layer; and

III) the upper SOI silicon layer to form a patterned first top dummy layer /top oxide layer /upper SOI silicon layer stack having exposed side walls; the patterned upper SOI silicon layer including a source region and a drain region connected by a channel portion;

e) forming a rounded oxide layer over the exposed side walls of the patterned upper SOI silicon layer;; the formation of the rounded oxide layer also rounding the patterned upper SOI silicon layer;

f) removing the patterned first top dummy layer exposing the patterned top oxide layer;

g) forming a second patterned dummy layer over the exposed patterned top oxide layer and the exposed portions of the upper SOI silicon layer; the second patterned dummy layer having an opening that defines a gate area exposing; the second patterned dummy layer being comprised of nitride or silicon nitride;

I) a portion of the oxide layer within the gate area;

II) portions of the upper surface of the lower SOI oxide layer within the gate area; and

III) a portion of the rounded oxide layer within the gate area;

h) etching the exposed gate area portions of the upper surface of the lower SOI oxide layer into the lower SOI oxide layer to:

I) form an undercut into the undercut lower SOI oxide layer exposing a bottom portion of the patterned upper SOI silicon layer within the gate area;

II) remove the exposed gate area portion of the oxide layer exposing a top portion of the patterned upper SOI silicon layer within the gate area; and

III) remove the portion of the rounded oxide layer within the gate area exposing a portion of the side walls of the patterned upper SOI silicon layer within the gate area;

i) forming a conformal oxide layer over:

I) the exposed bottom portion of the patterned upper SOI silicon layer within the gate area;

II) the exposed top portion of the patterned upper SOI silicon layer within the gate area; and

III) the exposed portion of the side walls of the patterned upper SOI silicon layer within the gate area;

j) forming a gate within the second patterned dummy layer opening; the gate including an upper gate above the patterned upper SOI silicon layer 14' within the gate area and a lower gate under the upper SOI silicon layer within the gate area; the gate being comprised of polysilicon; and

k) removing the second patterned dummy layer to form the double-gated transistor.

35. The method of claim 34, wherein the structure is a semiconductor substrate.

36. The method of claim 34, wherein the structure is comprised of silicon or germanium.

37. The method of claim 34, wherein the lower SOI oxide layer has a thickness of from about 1000 to 5000Å; the upper SOI silicon layer has a thickness of from about 300 to 2000Å; the first dummy layer has a thickness of from about 450 to 1050Å; the top oxide layer has a thickness of from about 90 to 110Å; the rounded oxide layer has a thickness of from about 80 to 550Å; the second patterned dummy layer has a thickness of from about 1000 to 3000Å; and the conformal oxide layer has a thickness of from about 5 to 200Å.

38. The method of claim 34, wherein the lower SOI oxide layer has a thickness of from about 2000 to 4000Å; the upper SOI silicon layer has a thickness of from about 500 to 1500Å; the first dummy layer has a thickness of from about 500 to 1000Å; the top oxide layer has a thickness of from about 95 to 105Å; the rounded oxide layer has a thickness of from about 100 to 500Å; the second patterned dummy layer has a thickness of from about 1500 to 2500Å; and the conformal oxide layer has a thickness of from about 10 to 50Å.

39. The method of claim 34, wherein the undercut is from about 500 to 3000Å deep.

40. The method of claim 34, wherein the undercut is from about 1000 to 2000Å deep.

41. The method of claim 34, wherein the undercut protrudes from about 500 to 3000Å under the second patterned dummy layer opening.

42. The method of claim 34, wherein the undercut protrudes from about 500 to 1000Å under the second patterned dummy layer opening.

43. The method of claim 34, wherein the patterned first dummy layer is removed using a hot phosphoric acid etch the undercut is formed using a dilute HF etch and the second patterned dummy layer is removed using hot phosphoric acid.

44. The method of claim 34, wherein the rounded oxide layer and the conformal oxide layer are each formed by a growth process.

45. The method of claim 34, including the step of forming source/drain implants into the respective source region and the drain region to form a source and a drain after removal of the second patterned dummy layer.

46. The method of claim 34, including the step of performing:

LDD implants; and

source/drain implants

after removal of the second patterned dummy layer.

47. The method of claim 34, wherein the upper gate has exposed side walls and including the step of forming spacers over the upper gate exposed side walls after removal of the second patterned dummy layer.

48. The method of claim 34, including the further step of then performing a salicidation process.